UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,492	08/20/2001	David R. Hembree	00-0625.1	6973

22823 7590 08/12/2004

STEPHEN A GRATTON
THE LAW OFFICE OF STEVE GRATTON
2764 SOUTH BRAUN WAY
LAKEWOOD, CO 80228

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/933,492	HEMBREE ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *52 - 66 and 70 - 77* is/are pending in the application.

4a) Of the above claim(s) *63 - 66* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *52 - 62 and 70 - 77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/5/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 5, 2004 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on May 27, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 52 – 54, 60 – 62, 71 – 74, 76 and 77 are rejected under 35 U.S.C. 102(b) as being anticipated by Farnworth et al. (U.S. Pat. No. 6,093,933).

Regarding claims 52, 53 and 60, Farnworth et al. discloses in e.g., Fig. 3, column 2, lines 33 - 48 and column 3, lines 8 – 25 a semiconductor component comprising:

- a substrate (semiconductor wafer 10) comprising a plurality of tested semiconductor components (semiconductor IC dice 12; column 3, lines 8 – 11) including a plurality of component contacts (pads on the die to connect the conductive paths 32) and a plurality of integrated circuits (Integrated circuits are inherently in the IC dice 12) in electrical communication with the component contacts (any integrated circuits that are electrically connected to the pads on the die), the components including at least one defective component (bad dice; column 3, lines 8 – 25);
- a metal layer (metal lines 32; column 2, lines 46 – 48) on the substrate comprising a plurality of conductors (at the connecting area on the elements 32) in electrical communication with the component contacts (see Fig. 3) configured to redistribute patterns of the component contacts into selected patterns, and to repair the defective component by connecting selected component contacts on the defective component with selected integrated circuits on the defective component (column 3, lines 16 – 25), and to reconfigure the component contacts on the defective component (claim 60; column 3, lines 16 – 25); and
- the components include a second defective component (a second bad die from the bad dies; column 3, line 11) and the conductors are configured to electrically isolate the second defective component (claim 53; column 3, lines 8 – 15).

Regarding claim 54, Farnworth et al. discloses in e.g., Fig. 3 the components (12) including a second defective component (a second bad die from the bad dies; column 3, line 11) and the conductors (at the connecting area on the elements 32) being configured to reconfigure the component contacts on the second defective component (column 3, lines 16 – 25).

Regarding claim 61, Farnworth et al. discloses in e.g., Fig. 3 a plurality of terminal contacts (pads on the die that connect the conductive paths 32) on the components in the selected patterns in electrical communication with the conductors.

Regarding claims 62 and 76, Farnworth et al. discloses in e.g., Fig. 3 the substrate comprising a semiconductor wafer (10) or portion thereof and the components (semiconductor dice) comprising a semiconductor dice.

Regarding claim 71, Farnworth et al. discloses in e.g., Fig. 3 the terminal contacts (pads on the die that connect the conductive paths 32) comprising balls or bumps and the second pattern comprising a grid array (see Fig. 3).

Regarding claim 72, Farnworth et al. discloses in e.g., Fig. 3 the contacts (pads on the die that connect the conductive paths 32) comprising bond pads.

Regarding claim 73, Farnworth et al. discloses in e.g., Fig. 3 the conductors (at the connecting area on the elements 32) fanning out from the first pattern to the second pattern.

Regarding claim 74, Farnworth et al. discloses in e.g., Fig. 3 the component (semiconductor dice 12) being contained on a substrate (a semiconductor wafer 10).

Regarding claim 77, Farnworth discloses in e.g., Fig. 3 and column 3, lines 8 – 25 the components including a second defective component and the conductors being configured to electrically isolate the second defective component.

5. Claims 56 – 59 and 70 are rejected under 35 U.S.C. 102(b) as being anticipated by Dasse et al. '273.

Regarding claims 56 and 70, Dasse et al. discloses in e.g., Fig. 2, column 3, lines 55 – 63 and column 11, lines 32 - 47 a semiconductor component comprising:

- a substrate (20) comprising a plurality of tested components (e.g., the elements 24 - 32) comprising a plurality of component contacts (see Fig. 3) in a plurality of patterns;
- the components (e.g., the elements 22 and 24 - 32) including a plurality of good components (e.g., any one of the elements 22, 24 - 27 and 29 - 32) and at least one defective component (28), each component comprising a plurality of contacts in first patterns, a plurality of integrated circuits in electrical communication with the contacts (claim 70, see Fig. 3);
- a plurality of terminal contacts on the components in a second patterns (claim 70, see Fig. 3); and
- a metal redistribution layer (44; column 4, line 7) on the substrate comprising a plurality of conductors (e.g., 45) configured to redistribute the first patterns to the second patterns of the component contacts (88 one of the elements 24 - 27 and 29 - 32) into selected patterns, and to electrically isolate the defective component (column 11, lines 32 – 35) on the substrate during burn-in testing

of the good components (column 3, lines 55 – 63), and to electrically connect multiple components in a cluster that excludes the defective component (Since the cluster (514) in e.g., Fig. 14 and Fig. 15 of Dasse et al. does not include any defective component, hence Dasse et al. discloses this limitation).

Since the element 45 of Dasse et al. is connected to a current limiting resistor 77 which isolating one or more defective die 28 from a wafer conductor, the element 45 electrically isolates the defective components to contact on the good components. Therefore, Dasse et al. discloses the following limitation "a metal layer ... [to] electrically isolate the defective component".

Regarding claim 57, Dasse et al. discloses in e.g., Fig. 2 and column 11, lines 32 – 35 a plurality of terminal contacting on the good components in the selected patterns in electrical communication with the conductors.

Regarding claim 58, Since the cluster (514) in e.g., Fig. 14 and Fig. 15 of Dasse et al. does not include any defective component, hence Dasse et al. discloses the conductors being configured to electrically connect a plurality of good components in a cluster (514) that exclude the defective component.

Regarding claim 59, Dasse et al. discloses in e.g., Fig. 2 the substrate (20) comprising a semiconductor wafer, and the components (22) comprising semiconductor dice or semiconductor packages.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 55 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. in view of Dasse et al. '273.

Regarding claim 55, Farnworth et al. discloses a second defective component. However, Farnworth et al. does not disclose the conductors being configured to electrically connect multiple components in a cluster that excludes the second defective component. Since the cluster (514) in e.g., Fig. 14 and Fig. 15 of Dasse et al. does not include any defective component, hence Dasse et al. teaches conductors (520) being configured to electrically connect multiple components (integrated circuit die) in a cluster (514) that excludes a defective component. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Farnworth et al. by using the conductors as taught by Dasse et al. The ordinary artisan would have been motivated to modify Farnworth et al. in the manner described above for at least the purpose of coupling to the integrated circuits in the cluster (column 25, lines 23 ~ 27).

8. Claim 75 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. in view of Farnworth (U.S. Pat. No. 5,851,911).

Regarding claim 77, Farnworth et al. discloses the claimed invention except for a protective layer on the conductors having a plurality of openings for the terminal contacts. However, Farnworth discloses in e.g., Fig. 3 a protective layer (1018) on conductors (1016) having a plurality of openings (1026) for terminal contacts (1032). Thus, it would have been obvious to one of ordinary skill in the art at the time when the

invention was made to modify Farnworth et al. by using the protective layer as taught by Farnworth. The ordinary artisan would have been motivated to modify Farnworth et al. in the manner described above for at least the purpose of protecting the circuits on the components from external environment such as water in the air.

Response to Arguments

9. Applicant's arguments with respect to claims 52 ~ 62 and 70 ~ 77 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
August 05, 2004

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800